19-1398; Rev 4; 5/07

EVALUATION KIT AVAILABLE

Upstream CATV Amplifier

General Description

The MAX3510 is a programmable power amplifier for use in CATV upstream applications. The device outputs up to 64dBmV (continuous wave) through a 2:1 (voltage ratio) transformer. It features variable gain controlled by a 3-wire digital serial bus. Gain control is available in 1dB steps. The device operates over a frequency range of 5MHz to 65MHz.

The MAX3510 offers a transmit-disable mode, which places the device in a high-isolation state for use between bursts in TDMA systems. In this mode the output stage is shut off, minimizing output noise. When entering and leaving transmit-disable mode, transients are kept to 7mV nominal at full gain. In addition, supply current is reduced to 25mA.

Two power-down modes are available. Software-shutdown mode permits power-down of all analog circuitry while maintaining the programmed gain setting. Shutdown mode disables all circuitry and reduces current consumption to less than 10µA.

The MAX3510 is available in a 20-pin QSOP package for the extended-industrial temperature range (-40°C to +85°C).

Applications

Cable Modems

CATV Set-Top Boxes

Telephony-Over-Cable

CATV Status Monitors

Features

- ♦ **Ultra-Low Power-Up/Down Transients, 7mV Typical at 59dBmV Output**
- ♦ **Single +5V Supply**
- ♦ **Output Level Ranges from <8dBmV to 64dBmV**
- ♦ **Gain Programmable in 1dB Steps**
- ♦ **Low Transmit Output Noise Floor: -47dBmV (160kHz BW)**
- ♦ **Low Transmit-Disable Output Noise: -70dBmV**
- ♦ **Two Power-Down Modes**

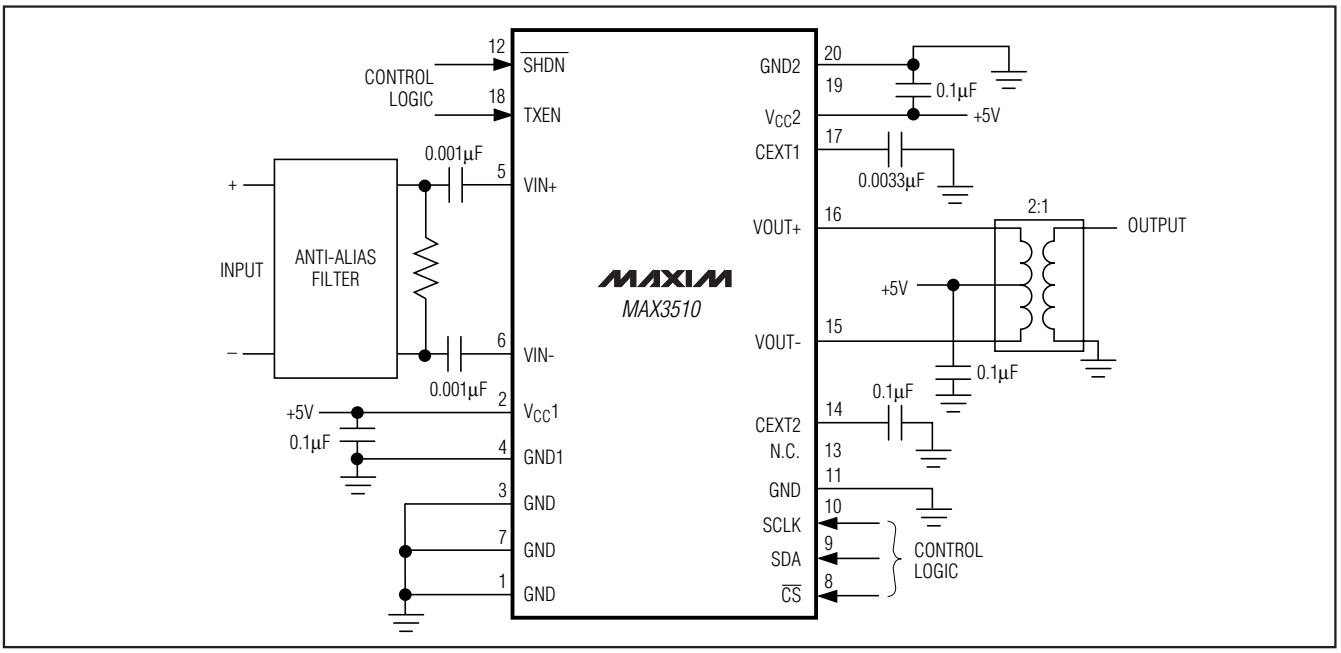
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3510EEP	-40°C to +85°C	20 QSOP
MAX3510EEP+	-40°C to +85°C	20 QSOP

+Denotes lead-free package.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} ($V_{CC}1$, $V_{CC}2$), VOUT+, VOUT- ..... -0.5V to +10.0V
Input Voltage Levels (all inputs),
CEXT1, CEXT2.....-0.3V to (V_{CC} + 0.3V)
Continuous Input Voltage (VIN+, VIN-) .....$2V_{P-P}$
Continuous Current (VOUT+, VOUT-).....80mA

Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate at 12.3mW/°C above +70°C)....1067mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, TXEN = $\overline{SHDN}$ = high, D7 = 1, T_A = -40°C to +85°C, unless otherwise noted. No input signal applied. Typical parameters are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75		5.25	V
Supply Current Transmit Mode	I_{CC}			109	126	mA
Supply Current Transmit-Disable Mode	I_{CC}	TXEN = low		26	30	mA
Supply Current Software-Shutdown Mode	I_{CC}	TXEN = low, D7 = 0 (Note 3)		1.4		mA
Supply Current Shutdown Mode	I_{CC}	$\overline{SHDN}$ = low, TXEN = low		1		µA
Input High Voltage	V_{INH}	T_A = 25°C	2.0			V
Input Low Voltage	V_{INL}	T_A = 25°C			0.8	V
Input High Current	I_{BIASH}	(Note 3)			100	µA
Input Low Current	I_{BIASL}	(Note 3)	-100			µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, TXEN = $\overline{SHDN}$ = high, D7 = 1, V_{IN} = 34dBmV differential, output impedance = 75Ω through a 2:1 transformer, T_A = -40°C to +85°C, unless otherwise noted. Typical parameters are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Gain	A_V	f_{IN} = 5MHz to 42MHz (Note 3)	Gain-control word = 1, T_A = -40°C to +85°C			-26	dB
			Gain-control word = 63, T_A = 0°C to +85°C	27			
			Gain-control word = 63, T_A = -40°C to 0°C	26			
		f_{IN} = 10MHz (Note 3)	Gain-control word = 50, T_A = -40°C to +85°C	16.7		20.4	
Bandwidth	f_{3dB}	V_{OUT} = 60dBmV, -3dB (Note 1)		84	100		MHz
Gain Rolloff (Notes 1, 2)		V_{OUT} = 60dBmV, f_{IN} = 42MHz			-0.9	-1	dB
		V_{OUT} = 60dBmV, f_{IN} = 65MHz			-1.6	-1.8	
1dB Compression Point	P1dB	A_V = 26dB, 42MHz (Note 1)		18.0	20.0		dBm
Output Step Size		f_{IN} = 5MHz to 42MHz (Note 3)	A_V = -26dB to +27dB, T_A = -0°C to +85°C	0.6	1	1.4	dB
			A_V = -26dB to +26dB, T_A = -40°C to 0°C	0.6	1	1.4	

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.25V, TXEN = $\overline{SHDN}$ = high, D7 = 1, V_{IN} = 34dBmV differential, output impedance = 75Ω through a 2:1 transformer, T_A = -40°C to +85°C, unless otherwise noted. Typical parameters are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Transmit Mode Noise (Note 1)		BW = 160kHz, A_V = 26dB				-78	dBc
		BW = 160kHz, A_V = -26dB			47	-46	dBmV
Transmit-Disable Mode Noise Floor		TXEN = low, BW = 160kHz, A_V = +26dB, f_{IN} = 5MHz to 65MHz (Note 1)				-70	dBmV
Isolation in Transmit-Disable Mode		TXEN low, gain control word = 61, f_{IN} = 65MHz		36	45		dB
TXEN Transient Duration		TXEN rise/fall time < 0.1µs, T_A = +25°C (Note 1)			3.2	5	µs
TXEN Transient Step Size (Note 1)		Gain = 26dB, T_A = +25°C			7	37	mV_{P-P}
		Gain = 2dB or lower, T_A = +25°C			0.7	3.7	
Input Impedance	$\lvert Z_{IN} \rvert$	f_{IN} = 5MHz to 65MHz, single-ended, T_A = +25°C (Note 1)		1.4	1.5		kΩ
Output Impedance	Z_{OUT}				75		Ω
Output Return Loss in Transmit Mode	R_L	f_{IN} = 5MHz to 65MHz (Note 1)	T_A = 0°C	8.0	13.5		dB
			T_A = +25°C	8.7	13.5		
			T_A = +85°C	8.9	13.9		
Output Return Loss in Transmit-Disable Mode	R_L	TXEN = low, f_{IN} = 5MHz to 65MHz (Note 1)	T_A = 0°C	7.1	12.0		dB
			T_A = +25°C	7.7	12.2		
			T_A = +85°C	9.7	12.7		
Two-Tone Third-Order Distortion (Note 1)	IM3	Input tones at 40MHz and 40.2MHz, V_{IN} = 28dBmV/tone, V_{OUT} = +54dBmV/tone, T_A = +25°C			-56	-53	dBc
		Input tones at 65MHz and 65.2MHz, V_{IN} = 28dBmV/tone, V_{OUT} = 53dBmV/tone, T_A = +25°C			-54	-51	
2nd Harmonic Distortion	HD2	f_{IN} = 33MHz, (Note 3) T_A = -40°C to +85°C	V_{OUT} = +54dBmV		-59	-53	dBc
			V_{OUT} = +59dBmV		-55	-50	
		f_{IN} = 65MHz, V_{OUT} = +59dBmV, T_A = +25°C (Note 1)			-54	-50	
3rd Harmonic Distortion	HD3	f_{IN} = 22MHz, T_A = -40°C to +85°C	V_{OUT} = +54dBmV		-58	-53	dBc
			V_{OUT} = +59dBmV		-54	-50	
		f_{IN} = 65MHz, V_{OUT} = +59dBmV, T_A = +25°C (Note 1)			-49	-44	
AM to AM	AM/AM	A_V = 26dB, V_{IN} swept from 34dBmV to 38dBmV (Note 1)			0.1		dB
AM to PM	AM/PM	A_V = 26dB, V_{IN} swept from 34dBmV to 38dBmV (Note 1)			1		degrees

TIMING CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, TXEN = $\overline{SHDN}$ = high, D7 = 1, T_A = +25°C, unless otherwise noted.)

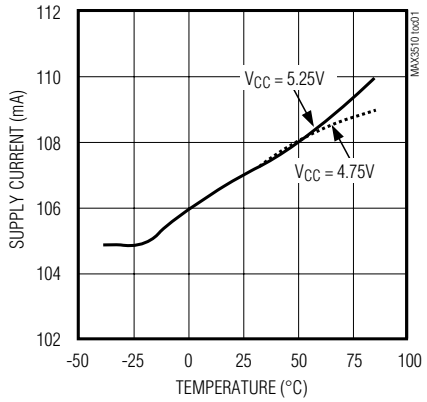
PARAMETER	SYMBOL	COMMENT	MIN	TYP	MAX	UNITS
$\overline{CS}$ to SCK Rise Setup Time	t_{SENS}		10			ns
$\overline{CS}$ to SCK Rise Hold Time	t_{SENH}		20			ns
SDA to SCK Setup Time	t_{SDAS}		10			ns
SDA to SCK Hold Time	t_{SDAH}		20			ns
SDA Pulse-Width High	t_{DATAH}		50			ns
SDA Pulse-Width Low	t_{DATAL}		50			ns
SCK Pulse-Width High	t_{SCKH}		50			ns
SCK Pulse-Width Low	t_{SCKL}		50			ns

Note 1: Guaranteed by design and characterization.
Note 2: Reference to 5MHz.
Note 3: Parameters <25°C guaranteed by design and characterization ±3.

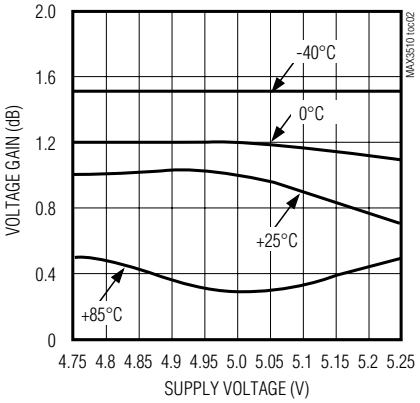
Typical Operating Characteristics

(V_{CC} = +5V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = high, f_{IN} = 20MHz, Z_{LOAD} = 75Ω through a 2:1 transformer, T_A = +25°C, unless otherwise noted.)

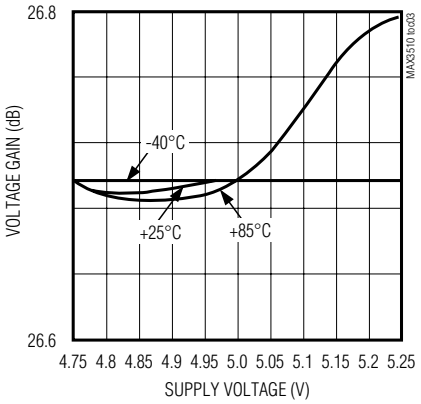
SUPPLY CURRENT vs. TEMPERATURE



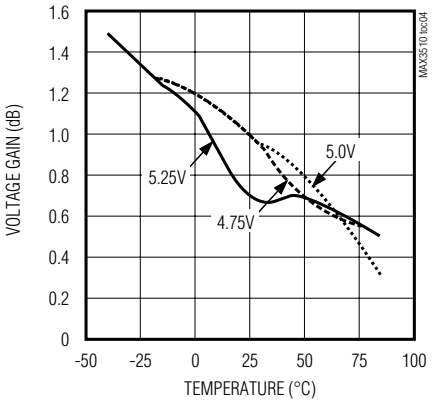
VOLTAGE GAIN vs. SUPPLY VOLTAGE (GAIN STATE = 33)



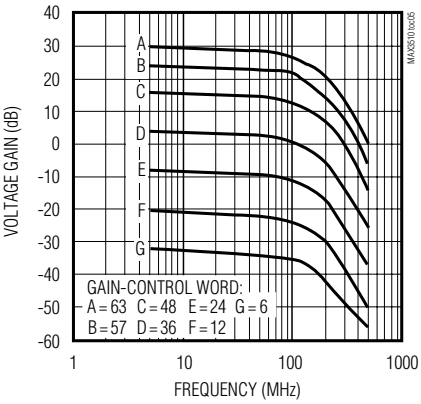
VOLTAGE GAIN vs. SUPPLY VOLTAGE (GAIN STATE = 60)



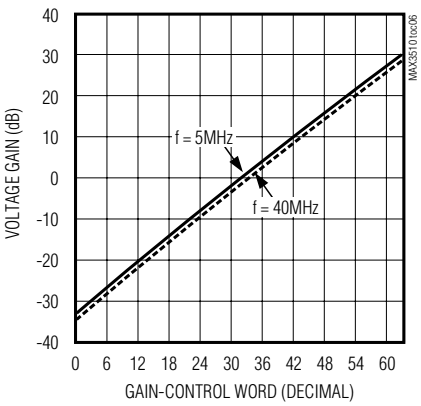
VOLTAGE GAIN vs. TEMPERATURE (GAIN STATE = 33)



VOLTAGE GAIN vs. FREQUENCY



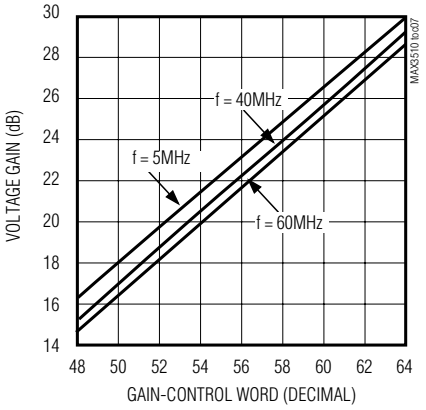
VOLTAGE GAIN vs. GAIN-CONTROL WORD



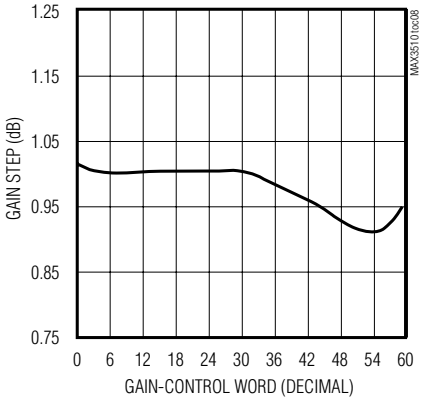
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{IN} = +34dBmV, TXEN = $\overline{SHDN}$ = high, f_{IN} = 20MHz, Z_{LOAD} = 75Ω through a 2:1 transformer, T_A = +25°C, unless otherwise noted.)

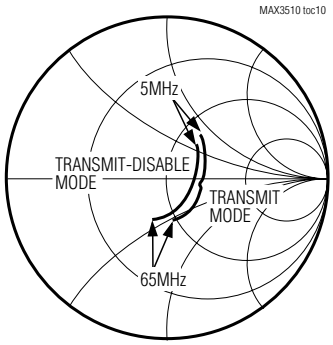
VOLTAGE GAIN vs. GAIN-CONTROL WORD



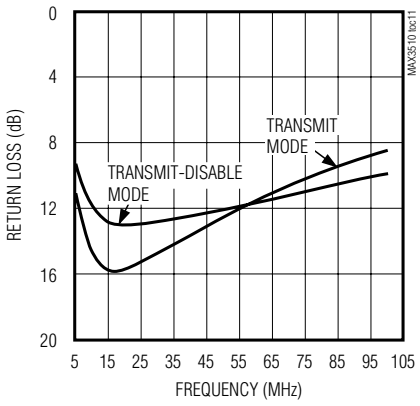
GAIN STEP vs. GAIN-CONTROL WORD



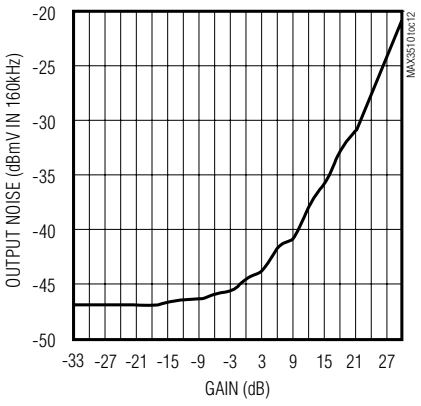
OUTPUT IMPEDANCE (75Ω REFERENCE)



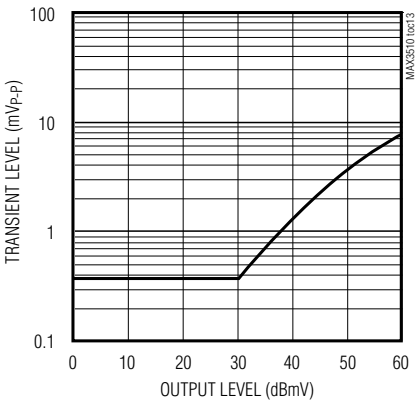
OUTPUT RETURN LOSS vs. FREQUENCY



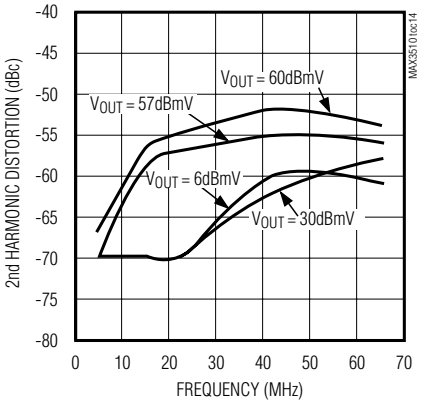
TRANSMIT OUTPUT NOISE vs. GAIN



POWER-UP/POWER-DOWN TRANSIENTS vs. OUTPUT LEVEL



2nd HARMONIC DISTORTION vs. INPUT FREQUENCY AND OUTPUT LEVEL



3rd HARMONIC DISTORTION vs. INPUT FREQUENCY

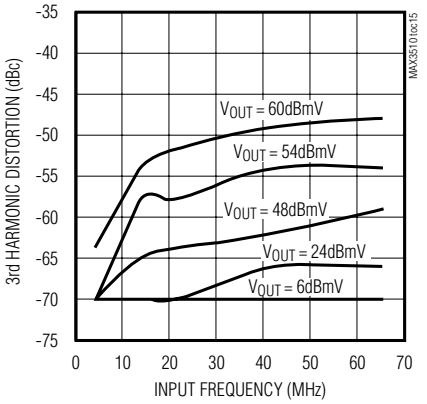


Table 1. Reflection Coefficients (75Ω reference)

FREQUENCY	TRANSMIT MODE		TRANSMIT MODE		TRANSMIT DISABLE MODE	
MHz	REAL S11	IMAG S11	REAL S22	IMAG S22	REAL S22	IMAG S22
1	0.937	-0.006	-0.494	0.625	-0.509	0.623
2	0.937	-0.007	-0.054	0.550	-0.075	0.577
5	0.936	-0.005	0.196	0.199	0.219	0.257
10	0.932	-0.011	0.183	0.017	0.244	0.062
20	0.932	-0.018	0.143	-0.081	0.219	-0.052
30	0.932	-0.026	0.108	-0.149	0.194	-0.121
40	0.927	-0.033	0.059	-0.199	0.158	-0.175
60	0.922	-0.054	-0.060	-0.257	0.066	-0.252
80	0.913	-0.075	-0.197	-0.252	-0.049	-0.284
120	0.889	-0.145	-0.420	-0.070	-0.281	-0.207
160	0.850	-0.249	-0.442	0.256	-0.409	0.037
200	0.753	-0.408	-0.212	0.543	-0.327	0.345

Pin Description

PIN	NAME	FUNCTION
1, 3, 7, 11	GND	Ground Pins
2	$V_{CC}1$	Programmable-Gain Amplifier (PGA) +5V Supply. Bypass this pin to GND1 with a decoupling capacitor as close to the part as possible.
4	GND1	PGA RF Ground. As with all ground connections, maintain the shortest possible (low-inductance) length to the ground plane.
5	VIN+	Positive PGA Input. Along with VIN-, this port forms a high-impedance differential input to the PGA. Driving this port differentially will increase the rejection of second-order distortion at low output levels.
6	VIN-	Negative PGA Input. When not used, this port must be AC-coupled to ground. See VIN+.
8	$\overline{CS}$	Serial-Interface Enable. TTL-compatible input. See the *Serial Interface* section.
9	SDA	Serial-Interface Data. TTL-compatible input. See the *Serial Interface* section.
10	SCLK	Serial-Interface Clock. TTL-compatible input. See the *Serial Interface* section.
12	$\overline{SHDN}$	Shutdown. When this pin and TXEN (pin 18) are set low, all functions (including the serial interface) are disabled, leaving only leakage currents to flow.
13	N.C.	No Connection
14	CEXT2	RF Output Bypass. This pin must be bypassed to ground with a 0.1µF capacitor.
15	VOUT-	Negative Output. Along with VOUT+, this port forms a 300Ω impedance output. This port is matched to a 75Ω load using a 2:1 transformer.
16	VOUT+	Positive Output. See VOUT-.
17	CEXT1	Transmit-Disable (Enable) Timing Capacitor. See the *Ramp Generator* section.
18	TXEN	Power-Amplifier Enable. Setting this pin low shuts off the power amplifier.
19	$V_{CC}2$	Power Amplifier Bias, +5V Supply. Bypass this pin to GND2 with a decoupling capacitor as close to the part as possible.
20	GND2	Power Amplifier Bias Ground. As with all ground connections, maintain the shortest possible (low inductance) length to the ground plane.

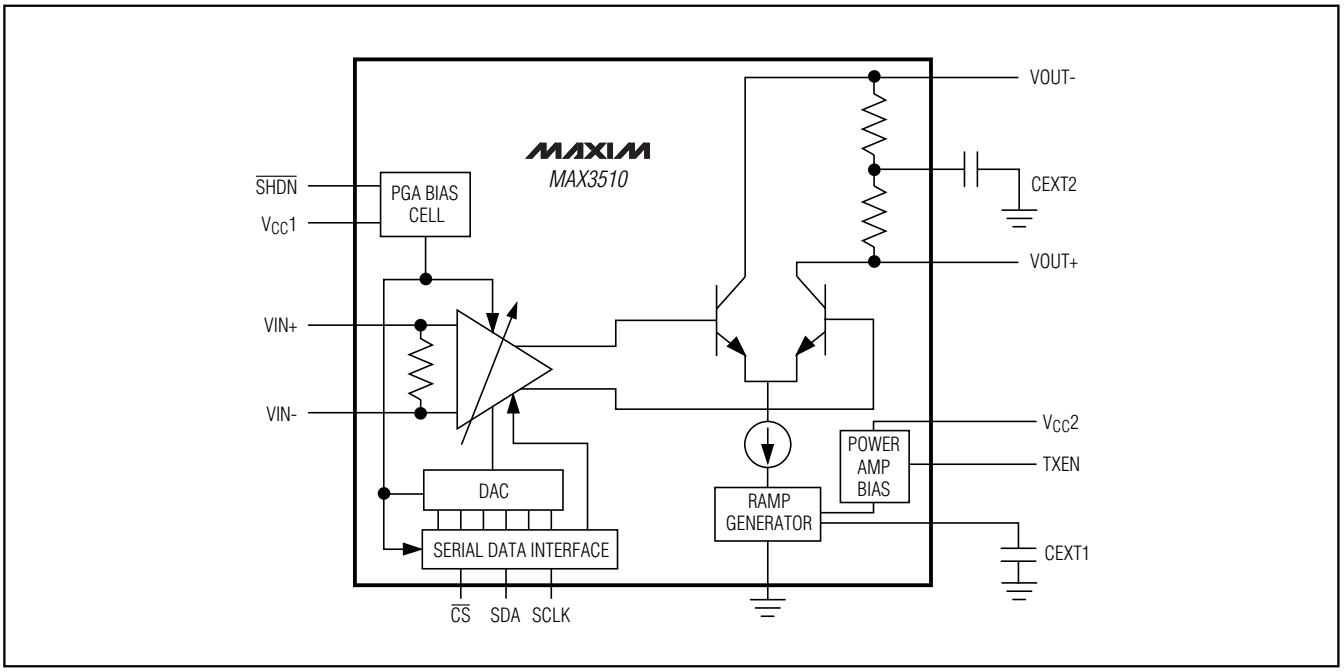


Figure 1. Functional Diagram

Detailed Description

The following sections describe the blocks shown in the functional diagram (Figure 1).

Programmable-Gain Amplifier

The programmable-gain amplifier (PGA) consists of the variable-gain amplifier (VGA) and the digital-to-analog converter (DAC), which provide better than 52dB of output level control in 1dB steps.

The PGA is implemented as a programmable Gilbert-cell attenuator. It uses a differential architecture to achieve maximum linearity. The gain of the PGA is determined by a 6-bit word (D5–D0) programmed through the serial data interface (Tables 2 and 3).

Specified performance is achieved when the input is driven differentially. The device may be driven single-ended; however, a slight increase in even-order distortion may result at low output levels. To drive the device in this manner, one of the input pins must be capacitively coupled to ground. Use a capacitor value large enough to allow for a low-impedance path to ground at the lowest frequency of operation. For operation down to 5MHz, a 0.001µF capacitor is suggested.

Power Amplifier

The power amplifier is a Class A differential amplifier capable of driving +64dBmV differentially. This architecture provides superior even-order distortion performance but requires that a transformer be used to convert to a single-ended output. In transmit-disable mode, the power amplifier is shut off. An internal resistor is placed across the output, so that the output impedance remains matched when the amplifier is in transmit-disable mode. Disabling the output devices also allows the lowest standby noise.

To achieve the proper load line, the output impedance of the power amplifier is 300Ω differential. To match this output impedance to a 75Ω load, the transformer must have a turns ratio (voltage ratio) of 2:1 (4:1 impedance ratio).

The differential amplifier is biased directly from the +5V supply using the center tap of the output transformer. This provides a significant benefit when switching between transmit mode and transmit-disable mode. Stored energy due to bias currents will cancel within the transformer and prevent switching transients from reaching the load.

Upstream CATV Amplifier

Ramp Generator

The ramp generator circuit is a simple RC charging circuit, which is used to control power-up and power-down of the output power amplifier. It is made up of CEXT1 and an internal 2kΩ resistor. The choice of CEXT1 is governed by the period of the burst on/off cycle. CEXT1 must be small enough to fully charge/discharge within a burst. A typical value of CEXT1 is 0.0033µF.

Serial Interface

The serial interface has an active-low enable ($\overline{CS}$) to bracket the data, with data clocked in MSB first on the rising edge of SCLK. Data is stored in the storage latch on the rising edge of $\overline{CS}$. The serial interface controls the state of the PGA. Tables 2 and 3 show the register format. Serial-interface timing is shown in Figure 2.

PGA Bias Cell

The PGA bias cell is accessed by the $\overline{SHDN}$ pin. When this pin is taken low, the programmable-gain amplifier and serial data interface are shut off. Note that any gain setting stored in the serial data interface latch will be lost. The power amplifier is unaffected by the PGA Bias cell, therefore TXEN must be held low to be in shutdown mode. This mode lowers supply current draw to less than 1µA typical.

Power Amp Bias Cell

The power amp bias cell is used to enable and disable bias to the output differential pair. This is controlled by the TXEN pin (18).

Functional Modes

The MAX3510 has four functional modes controlled through the serial interface or external pins (Table 3): transmit mode, transmit-disable mode, software-shutdown mode, and shutdown mode.

Transmit Mode

Transmit mode is the normal active mode of the MAX3510. The TXEN pin must be held high in this mode. Note that $\overline{SHDN}$ must also be held high.

Transmit-Disable Mode

When in transmit-disable mode, the power amplifier is completely shut off. This mode is activated by taking TXEN low while keeping $\overline{SHDN}$ high. This mode is typically used between bursts in TDMA systems. Transients are controlled by the action of the transformer balance.

Software-Shutdown Mode

Software-shutdown mode is enabled when D7 = 0 and TXEN is low. This mode minimizes current consumption while maintaining the programmed gain state stored in the latch of the serial-data interface. All analog functions are disabled in this mode and current consumption is reduced to under 2mA.

Shutdown Mode

In normal operation the shutdown pin ($\overline{SHDN}$) is held high. When $\overline{SHDN}$ and TXEN are taken low, all circuits within the IC are disabled. Only leakage currents flow in this state. Data stored within the serial-data interface latches will be lost upon entering this mode. Current draw is reduced to 1µA (typ) in shutdown mode.

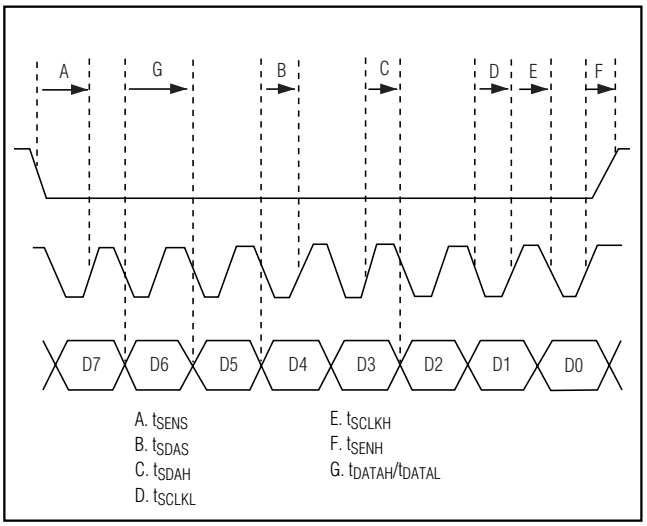


Figure 2. Serial-Interface Timing Diagram

Table 2. Serial-Interface Control Word

BIT	MNEMONIC	DESCRIPTION
MSB 7	D7	Software Shutdown
6	D6	Test Bit
5	D5	Gain Control, Bit 5
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit 0

Table 3. Chip-State Control Bits

$\overline{SHDN}$	TXEN	D7	D6	D5	D4	D3	D2	D1	D0	GAIN STATE (DECIMAL)	STATE
0	0	X	X	X	X	X	X	X	X	X	Shutdown Mode
1	0	0	X	X	X	X	X	X	X	X	Software-Shutdown Mode
1	0	1	X	X	X	X	X	X	X	X	Transmit-Disable Mode
1	1	1	X	X	X	X	X	X	X	X	Transmit Mode
1	1	1	X	0	0	0	0	0	0	0	Gain = -32dB*
1	1	1	X	0	0	0	0	0	1	1	Gain = -31dB*
1	1	1	X	—	—	—	—	—	—	—	—
1	1	1	X	1	0	0	0	0	0	32	Gain = 0dB*
1	1	1	X	—	—	—	—	—	—	—	—
1	1	1	X	1	1	1	1	1	0	62	Gain = 29dB*
1	1	1	X	1	1	1	1	1	1	63	Gain = 30dB*

**Typical gain at +25°C and V_{CC} = +5V*

Applications Information

Output Match

The MAX3510's output circuit is an open-collector differential amplifier. An on-chip resistor across the collectors provides a nominal output impedance of 300Ω in transmit mode and transmit disable mode.

Transformer

To match the output of the MAX3510 to a 75Ω load, a 2:1 (voltage ratio) transformer is required. This transformer must have adequate bandwidth to cover the intended application. Note that most RF transformers specify bandwidth with a 50Ω source on the primary and a matching resistance on the secondary winding. Operating in a 75Ω system will tend to shift the low-frequency edge of the transformer bandwidth specification up by a factor of 1.5, due to primary inductance. Keep this in mind when specifying a transformer.

Bias to the output stage is provided through the center tap on the transformer primary. This greatly diminishes the on/off transients present at the output when switching between transmit and transmit-disable modes. Commercially available transformers typically have adequate balance between half-windings to achieve substantial transient cancellation.

Finally, keep in mind that transformer core inductance varies proportionally with temperature. If the application requires low temperature extremes (less than 0°C), adequate primary inductance must be present to sustain low-frequency output capability as temperatures drop. In general this will not be a problem, as modern RF transformers have adequate bandwidth.

Input Circuit

To achieve rated performance, the input of the MAX3510 must be driven differentially with an appropriate input level. The differential input impedance is approximately 1.5kΩ. Most applications will require a differential lowpass filter preceding the device. The filter design will dictate terminating impedance of a specified value. Place this load impedance across the AC-coupled input pins (see *Typical Operating Circuit*).

The MAX3510 has sufficient gain to produce an output level of 60dBmV (CW through a 2:1 transformer) when driven with a 34dBmV input signal. Rated performance is achieved with this input level. When a lower input level is present, the maximum output level will be reduced proportionally and output linearity will increase. If an input level greater than 34dBmV is used, the 3rd-order distortion performance will degrade slightly.

If a single-ended source drives the MAX3510, one of the input terminals must be capacitively coupled to ground (VIN+ or VIN-). The value of this capacitor must be large enough to look like a short circuit at the lowest frequency of interest. For operation at 5MHz with a 75Ω source impedance, a value of 0.1µF will suffice.

Upstream CATV Amplifier

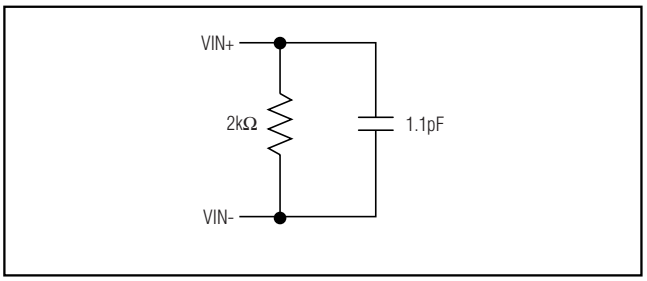


Figure 3. Equivalent Input Circuit

The model for the MAX3510 input impedance is shown in Figure 3.

Layout Issues

A well-designed printed circuit board is an essential part of an RF circuit. For best performance pay attention to power-supply layout issues as well the output circuit layout.

Output Circuit Layout

The differential implementation of the MAX3510's output has the benefit of significantly reducing even-order distortion, the most significant of which is 2nd-harmonic distortion. The degree of distortion cancellation depends on the amplitude and phase balance of the overall circuit. It is critical that the traces that lead from the output pins be exactly the same length.

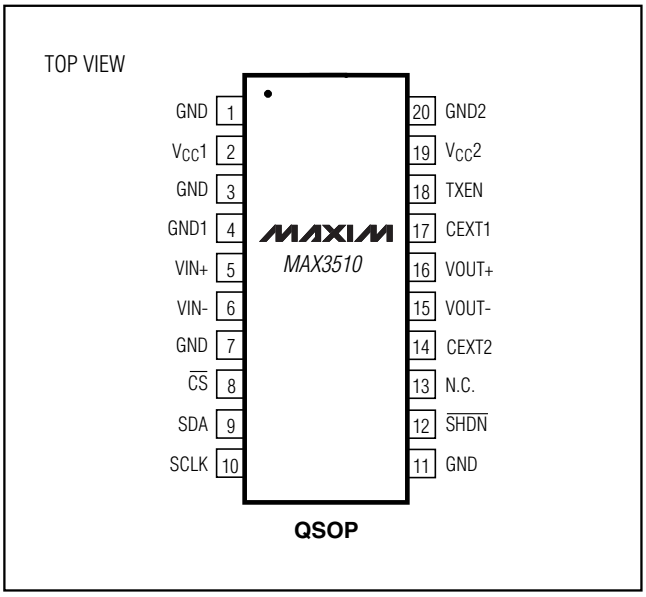
Power-Supply Layout

For minimal coupling between different sections of the IC, the ideal power-supply layout is a star configuration. This configuration has a large-value decoupling capacitor at the central power-supply node. The power-supply traces branch out from this node, each going to a separate power-supply node in the MAX3510 circuit. At the end of each of these traces is a decoupling capacitor that provides a very low impedance at the frequency of interest. This arrangement provides local power-supply decoupling at each power-supply pin.

The power supply traces must be made as thick as practical to keep resistance well below 1Ω.

Ground inductance degrades distortion performance. Therefore, ground plane connections to GND1 and GND2 should be made with multiple vias if possible.

Pin Configuration



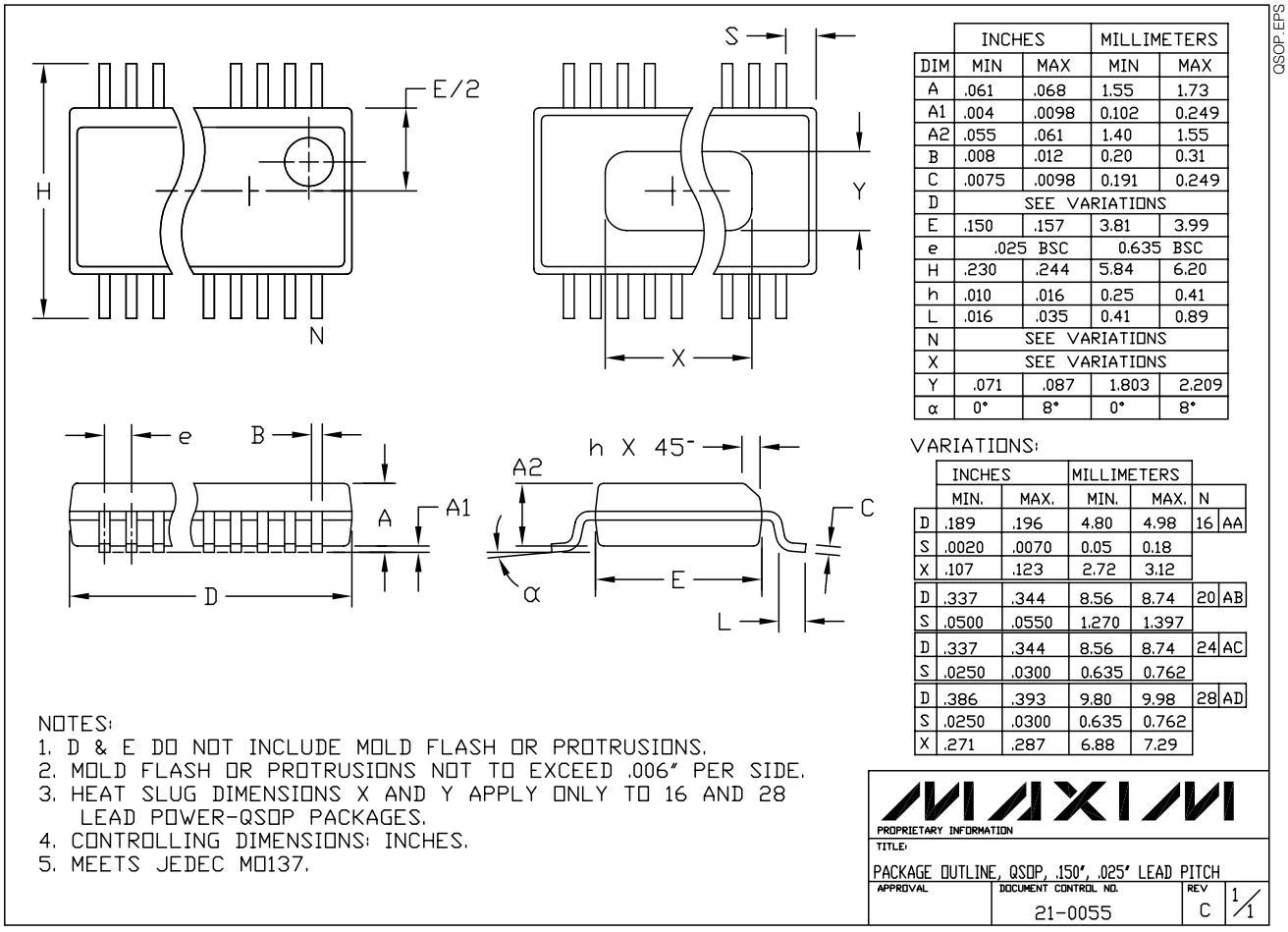
Chip Information

TRANSISTOR COUNT: 736

Upstream CATV Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

Revision History

Pages changed at Rev 4: 1, 2, 12